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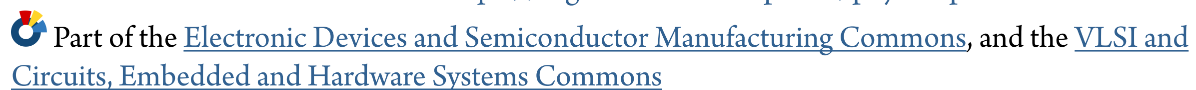
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On The Radiation-Induced Soft Error Performance of Hardened Sequential Elements in Advanced Bulk CMOS Technologies

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Abstract

Test chips built in a 32nm bulk CMOS technology consisting of hardened and non-hardened sequential elements have been exposed to neutrons, protons, alpha-particles and heavy ions. The radiation robustness of two types of circuit-level soft error mitigation techniques has been tested: 1) SEUT (Single Event Upset Tolerant), an interlocked, redundant state technique, and 2) a novel hardening technique referred to as RCC (Reinforcing Charge Collection). This work summarizes the measured soft error rate benefits and design tradeoffs involved in the implemented hardening techniques.

Neutron; Alpha particle; neutron; proton; heavy ion; space; terrestrial; single event effects; SEE; soft errors; SE; hardened;mitigation

Introduction

Ionizing radiation is known to cause noise bursts in silicon (Si) substrates of modern integrated circuits (ICs) [1-3]. If the amount of charge collected at reverse-biased junctions is larger than the so-called critical charge (Qcrit), an upset occurs [4]. Due to the relatively low flux rates in the radiation environments of interest in this work, faults are induced by single particles and all radiation induced phenomena are referred to as single event effects (SEE). In memory type cells radiation-induced faults are called single event upsets (SEU). SEUs are stable in time until the upset devices are re-written. An entirely different class of radiation-induced faults is formed by single event transients (SETs). SETs occur in static combinational logic where the node voltage is always restored in the case of a particle strike. Radiation induced glitches per se do not result in errors on the chip or system level until the glitch is captured by a receiving storage element [5]. SETs in clock networks are discussed in reference [6].

More than 95% of all upsets at sea-level are either due to a) high-energy neutrons, or b) alpha particles emitted from radioactive isotopes located within ~50µm of the active Si surface [3, 7]. In contrast, soft error upsets in a space environment mainly result from a) protons trapped in belts by earth's magnetosphere in the case of low earth orbits, and b) heavy ions in geosynchronous orbits. For a detailed description of the different radiation environments, please see reference [8].

Neutrons and high energy protons, in contrast to alpha particles or heavy ions, do not directly ionize Si but generate electron hole pairs via secondary ions that are created in nuclear reactions [2, 9]. There are two classes of nuclear collisions: elastic and inelastic scattering. In most elastic events, only a small amount of energy is transferred onto the target nucleus, which recoils but does not change its intrinsic energy state. In case of an inelastic event, secondary protons, neutrons, and pions are produced, and an excited intermediate nucleus is formed. This nucleus subsequently de-excites by the emission of other secondary particles, and it is finally transformed into a stable and lighter residual nucleus. The secondary fragments from the second reaction stage consist of protons, neutrons, light ions, and heavy residual nuclei. The heavy recoiling nuclei typically deposit a large amount of charge in a small volume, whereas the secondary light fragments deposit charge over path lengths that are large compared to typical device dimensions. Low-energy secondary protons deposit appreciable ionization energies (per unit track length) in the Si substrate. For modern technologies, characterized by low Qcrit values, these low energy protons might be a significant contributor to device upset rates through direct ionization rather than nuclear reactions [10].

If the radiation event deposits sufficient charge, more than a single device or bit may be affected, creating a so-called multi-cell upsets (MCU) as opposed to a single bit upsets (SBU) [11]. Technology scaling is known to increase the fraction of MCU clusters dramatically, with important implications for future memory architectures in systems utilizing error correction codes (ECC). Recent studies have demonstrated the increased sensitivity of memory type devices in the presence of MCU and charge sharing[1] for various radiation environments [11, 12, 13].

Most published SER trend data are for terrestrial environments. However, there is no reason why similar trends should not be expected for space applications. With process scaling, most authors agree that the total SER/bit is decreasing for SRAM devices [11, 14, 15, 16]. Because most SRAM arrays are nowadays protected, SRAM trends are becoming of lesser importance. This is in contrast to random logic, which is much more difficult and expensive to protect [17, 18]. No industry-wide agreement seems to exist for logic devices [3, 19, 20]. However, to the best of our knowledge, logic SER on the chip-level is expected to increase per generation if no additional mitigation techniques are implemented. MCU rates show an exponential increase with process scaling [11].

In a recent publication it was speculated that the return on investment of some popular design mitigation techniques that rely on separation in space, such as interleaving in memory arrays, or hardened devices utilizing local redundancy, might suffer greatly with continued process scaling [21]. For older technologies conventional radiation-hardened-by-design (RHBD) approaches such as Dual Interlocked Cell (DICE), Built-in Soft Error Resilience (BISER), Single Event Upset Tolerant (SEUT) or Triple Modular Redundancy designs (TMR) provide excellent protection against SEU [22, 23, 24, 25]. With technology scaling, charge collection at multiple nodes due to a single particle strike is becoming more probable. One of the key objectives of our work is to measure and characterize the SER benefit of mitigation techniques that rely on hardening by redundancy. To quantify the impact of scaling, the authors designed and implemented hardened devices with different minimum node separation design

[1] The term charge sharing is somewhat misleading. It denotes collection of charge by two or more nodes (within the same or different cells) due to the one particle strike (i.e., one single event).

rules on two test chips. The implemented and tested mitigation technique is SEUT [24]. However, the learning gained by this study is expected to be applicable to any circuit-level mitigation scheme that relies on separation in space of redundant state nodes. Experimental SER results for various radiation environments are presented. Another key objective of this work is to introduce and characterize the soft error sensitivity of a novel circuit level mitigation technique called RCC (Reinforcing Charge Collection). RCC promises very low power and area overheads at sufficiently low upset rates and most importantly is expected to show better technology scaling properties than redundancy based techniques.

TEST CHIP DESIGNS

Two different soft error (SE) test chips have been designed and built in a 32nm CMOS bulk technology. Each test chip (TC) contains thousands of instantiations of several flavors of sequential elements each, all chained together in a shift register fashion [24]. All relevant elements are briefly summarized in Table 1.

TABLE 1. SUMMARY OF TEST CHIPS AND IMPLEMENTED SEQUENTIAL DESIGNS.

Test Chip	Sequential Design	Description
TC1	Ref. Latch	Standard library reference latch
	SEUT800	SEUT latch with sensitive diffusion separation of about 800nm
	SEUT150	SEUT latch with sensitive diffusion separation of about 150nm
	RCC2	RCC latch with sensitive diffusion separation of 5 poly widths
	RCC1	RCC latch with one poly width diffusion separation
TC2	SEUT800	SEUT latch with sensitive diffusion separation of about 800nm
	SEUT600	SEUT latch with sensitive diffusion separation of about 600nm
	SEUT400	SEUT latch with sensitive diffusion separation of 400nm
	SEUT150	SEUT latch with sensitive diffusion separation of about 150nm

In the following sections, upset modes and key properties of each investigated design style (SEUT and RCC) will be explained.

Local Redundancy Hardened Designs

Many redundancy based hardened designs have been published and tested [22, 23, 24, 27, 28, 29, 30]. Formal design and analysis techniques have also been developed for SEU immune circuits [31, 32]. Most designs are single error correcting circuits except BISER [23]—which is an error blocking design. Single error correcting designs, such as SEUT [24, 30], recover upsets to a correct state after radiation induced pulse is removed without waiting for the next clock signal. Error blocking designs use two redundant memory elements and add error blocking logic at the output to block error propagation. BISER reuses scan circuits as redundant memory to reduce area and power penalties and a C-element at the output to block error propagation. SEUT and BISER devices as well as other redundancy based hardened designs such as TMR are expected to show very similar radiation properties and dependencies on circuit parameters such as critical state node separation, critical charge and diffusion areas [21].

Redundancy based hardened designs discussed in this work can only recover strikes when charge is collected by one node (with the exception of clock node strikes, see below). It is very important to separate "critical nodes" in space to minimize the amount of charge collected at those sensitive nodes. Therefore, SER reduction is strongly dependent on critical node spacing. The farther critical nodes are separated, the higher the SER reduction (see below). The flipside of larger spacing is larger cell areas. Hence, trade-offs must be made to balance SER reduction and cell area growth. Technology scaling reduces spacing by about ~0.7x each generation. This imposes a big challenge on hardened circuit design for current and future generation designs.

A second major upset mechanism of hardened sequential elements is clock node strikes [16]. Please note that this upset mechanism does not involve charge collection at more than one node and therefore can be a significant SER contributor. In principle one can distinguish two modes of clock node upsets [6]: a) Radiation-induced race which reflects a false opening of the receiving sequential and data racing through it. For non-critical paths this mode is the dominating clock node upset mechanism. b) Radiation-induced clock jitter, where the clock edge is shifted by the particle strike such that for critical paths, data will not be latched correctly. Due to the very slow clock speeds applied in our experiments, our shift register test chips were not sensitive to radiation-induced jitter.

Finally, for non error blocking schemes and strikes that yield transient glitches (SETs) only, pulses could propagate to downstream logic and could potentially be latched by downstream sequential elements—similar to other forms of noise in combinational logic. This soft error contributor of hardened sequential elements is difficult to quantify (by simulation or measurements), but nevertheless might become an important SER contributor in future technologies. However, our test chips are not sensitive to this upset mode due to the implemented design and test methodology.

The core design of all tested local redundancy hardened cells is the storage element shown in Figure 1, which replaces the classical cross-coupled inverter non-hardened memory element. The fully interrupted SEUT circuit features redundant data signals (d0 and d2) to reduce the overall cell SER[2]. During a normal write operation, clock is high and input passgates are on. The transistors controlled by clock inputs to SEUT are off. Data is written into SEUT inputs d0 and d2 which controls qp2, qn2, qp5 and qn5 setting states d1 and d3 correctly.

[2] Another option to reduce SER would be to protect clock nodes by implementing redundant clocks.

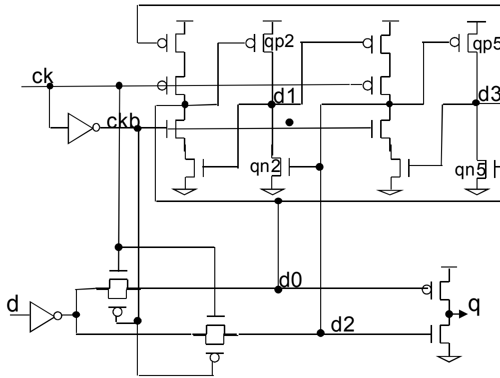

FIGURE 1. SEUT STORAGE CELL [24, 30]

Qcrit simulation results and a SER model of SEUT (and other local redundancy hardened designs) have been introduced and discussed in reference [21]. In the following, key findings are briefly summarized (see Figure 2).

The key innovation that differentiates the hardened circuit-level simulation methodology from traditional ones is that not one but two (or more) current sources are attached to the nodes that are simultaneously collecting charge [21]. One has to differentiate between charge collection at the primary and secondary nodes[3]: Qcrit of the primary node is simulated by iterating the collected charge at the primary node as a function of charge collected at the secondary node Qs until the circuit fails. Two distinct regions can be observed. At low Qs values Qcrit initially decreases steeply with increasing Qs. Therefore a Qs threshold exists below which the primary node cannot be upset, independent on how much charge is collected on the secondary node. In other words, a minimum amount of charge needs to be collected at the electrically coupled secondary node, or the device cannot be upset by charge sharing. The soft error rate under charge sharing conditions SER_{CS} then equals the integral over the product of the SBU soft error rate $SER(Qcrit_p(Qs(x))$ at the primary node p with P(Qs(x)|Qcrit(Qs(x))) [21, 33]

$$SER_{CS}(p,s,x) \propto \int_0^\infty \begin{array}{l} P(Q_s(x) \mid Qcrit_P(Q_s(x)))\, * \\ SER(Qcrit_p(Q_s(x))dQ_s \end{array} \qquad (1)$$

P(Qs(x)|Qcrit(Qs(x)))dQs[4] denotes the conditional probability that charge Q in the interval [Qs, Qs+dQs] is collected at the secondary node, given that Qcrit or more is collected at the primary node due to the same single event. The probability P(Qs(x)|Qcrit(Qs(x))) decreases steeply with node (actually diffusion) separation (x) which can be determined from layout [21]. The integrand in equation (1) P*SER contributes significantly only in a small Qs range due to the Qs dependence of P and the Qcrit(Qs) dependence of SER (see Figure 2) [21].

[3] Amusan calls the two charge collecting nodes active and passive [13].
[4] Old terminology is P(Q,x,A). Diffusion area dependence is dropped here for better readability.

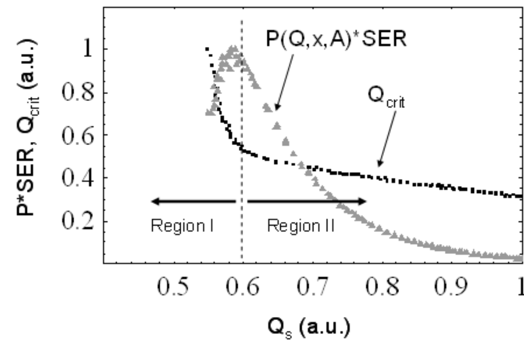

FIGURE 2. SEUT QCRIT AND P(Q,X,A) VS QS [21]

Reinforcing Charge Collection (RCC) Design

RCC is best explained using a static storage element, typically consisting of a pair of cross-coupled inverters. In each inverter, the OFF device's diffusion (referred to as victim diffusion) is vulnerable to collecting ionizing-particle-induced charge that can disrupt the stored state. The ON device's diffusion[5] (referred here as reinforcing diffusion), on the other hand, collects charge that reinforces the stored state (in the case of the RCC design at least). If the charge generated by a particle strike can be collected in both the victim and reinforcing diffusions (charge sharing), the critical charge (Qcrit) needed to upset the stored state can be increased, thus reducing SER.

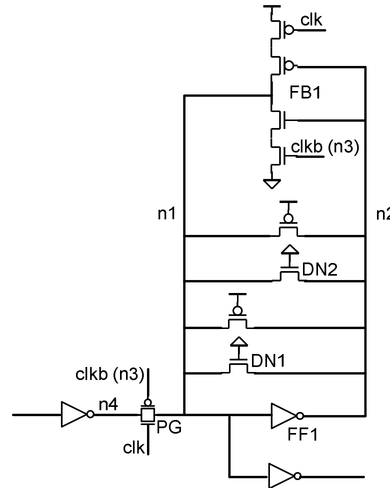

FIGURE 3. RCC SCHEMATIC

The victim diffusion is fully reverse biased making it an efficient collector of the particle-induced charge. The reinforcing diffusion initially has no externally applied reverse bias, but has only the built-in potential, making it a weak collector. However, even this weak collection serves to increase Qcrit [34]. Furthermore, once the victim diffusion begins collecting charge the electric field across the victim diffusion's depletion region quickly collapses [25]. Simultaneously, since the reverse bias across the reinforcing diffusion increases, its depletion region widens and the charge collection efficiency increas-

[5] I.e., ON during normal circuit operation when the particle strike occurs. In general charge collection that occurs simultaneously can be reinforcing or weakening. Both, victim and reinforcing diffusions can be primary or secondary nodes.

es. In modern day circuits, these field fluctuations occur in picosecond time scales. Therefore, charge collection in victim and reinforcing nodes is a highly dynamic process that requires mixed-mode device simulations to correctly model. Kawakami et al. [34] have published such simulations, and have shown the increase in Qcrit theorized here. However, they did not do these simulations in the context of radiation hardening. In this work, cells were specifically designed to maximize charge sharing, and Si test structures were used to show its effectiveness.

In order for charge sharing to occur, the victim and reinforcing nodes need to be physically close to each other (see equation 2 below). Typical layout of these cross-coupled structures might already have these nodes physically close to each other. However, test structure measurements show that if these nodes are within a minimum design rule dimension of each other, the closer proximity leads to a dramatic SER reduction. In this work, “dummy” gates (OFF transistors) have been used to bring the diffusions of the same type within one poly dimension. This greatly increases the probability that charge generated by a particle will be collected by both diffusions, thus reducing SER. Introduction of the dummy gates does cost leakage power. In addition, storage node capacitance and area will increase in most cases, since there is less opportunity for diffusion sharing in layout. This costs dynamic power. The impact of increased capacitance and area on SER can be simulated [36], and is shown later in Tables 3 and 5. Figure 3 is a RCC latch schematic that shows two pairs of dummy devices that are OFF, and whose sole purpose is to minimize victim-to-reinforcing diffusion separation. One pair allows charge sharing between victim and reinforcing diffusions of the cross-coupled inverters. The other pair allows charge sharing between the input pass gate diffusion and its complement node. The layout stick diagram for such an arrangement is shown in Figure 4. Only the N diffusions are shown; P diffusions have a similar arrangement.

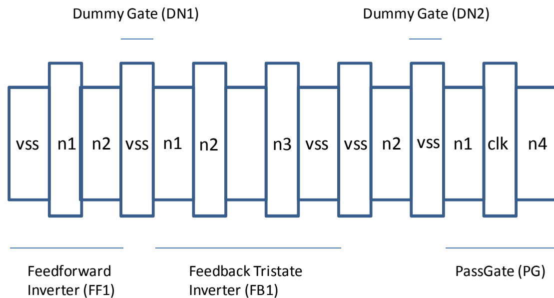

FIGURE 4. RCC LAYOUT DIAGRAM FOR N DIFFUSIONS

A test chip with the latch shown in Figure 3 was built in a 32nm technology (TC1; Table 1). The separation between victim and reinforcing nodes is one poly width for this cell. A cell with no dummy gates was also placed on the test chip. The minimum separation between victim and reinforcing nodes is increased in this version due to standard layout techniques that incorporate a shared power diffusion between critical diffusions (RCC2 in Table 1). The control latch has the same size devices as both RCC flavors implemented on TC1.

The SER of non-redundancy hardened devices under charge sharing conditions (CS), for nodes p (primary) and s (secondary) is given by [33]

$$\begin{aligned} &SER_{CS}(p,s) = SER(Qcrit_p(0)) + \Delta SER_{CS} \\ &\Delta SER_{CS}(p,s,x) = \\ &\propto \int_0^\infty \left[P(Q_s(x) \mid Qcrit_p(Q_s(x))) * \begin{pmatrix} SER(Qcrit_p(Q_s(x)) - \\ SER(Qcrit_p(0)) \end{pmatrix} \right] dQ_s \end{aligned} \quad (2)$$

where SER denotes the nominal soft error rate when charge sharing is ignored and ΔSER_{CS} the correction term in the presence of charge sharing. Symbols have the same meanings as in the previous section. Qcrit (0) denotes the critical charge of the primary node if only the primary node collects charge. It is important to realize that ΔSER_{CS} can be positive or negative depending on the node distances (x), states involved and diffusion types. P(Qs(x)|Qcrit(Qs(x))) is a steeply decreasing function with increasing Qs(x) and hence with increasing x. In the case of redundancy hardened devices the main design objective is to reduce SER by maximizing the separation (x) of nodes that increase Qcrit if simultaneous charge collection occurs[6]. In contrast, the key mitigation concept behind RCC devices is to minimize distances of diffusions of nodes that reinforce the stored state if charge is collected simultaneously.

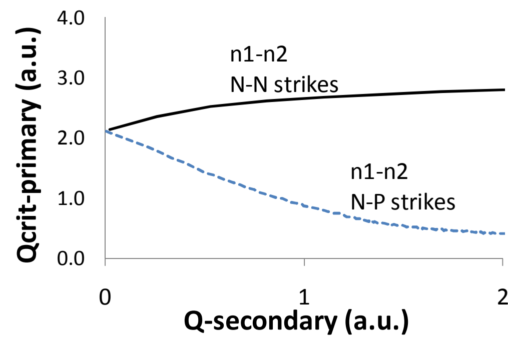

FIGURE 5. SIMULATED CRITICAL CHARGES OF A NON-HARDENED LATCH IN THE PRESENCE OF CHARGE SHARING BETWEEN NODES N1 AND N2.

There are, however, nodes that need to be kept separated even in the RCC design. For instance, N-N strikes (denoting NMOS strikes in the case of charge collecting nodes n1 and n2) result in an increase in critical charges and a correspondingly decrease in SER (solid line in Figure 5). N-P strikes in the same inverter can also decrease SER. In contrast, N-P strikes (denoting strikes where charge is collected in the OFF NMOS on one side and the OFF PMOS on the other side) results in an increase in SER (dashed line in Figure 5). For N-N strikes, one might wonder how it is possible that NMOS diffusions on both sides of the cross-coupled inverter collect charge simultaneously. One of the NMOS must be ON, and the junction therefore is not reversed biased. As explained earlier, the assumption behind equation (2) is that the radiation induced SET propagates turning off the NMOS on the other side allowing charge to be collected there efficiently during this time period. Logic in modern technologies is sufficiently fast and SETs sufficiently wide such that both NMOS on either side of the cross-coupled devices are reversed biased and charge is temporarily collected at nearly the same time. However, both devices are not off for equal lengths in time and equation (2) still needs to be adjusted and fitted to experimental or simulation data.

[6] The RCC concept can be combined with local redundancy schemes such as the one implemented in SEUT to achieve even better SER performance levels.

EXPERIMENTAL SETUP

Logic test vehicles built in a 32nm high-k + metal gate process [35] have been exposed to neutron, proton, alpha-particle and heavy ion radiation. The sensitivity of the test structures to alpha-particle radiation was studied by placing Thorium-232 foils on the wire bonded test chips described above. Neutron SER data were collected at the Los Alamos Laboratory Weapons Neutrons Research (WNR) facility, New Mexico (see Figure 6 for typical setup). Proton and heavy-ion irradiation experiments were conducted at the Indiana University Cyclotron facility (IUCF) and Texas A&M University facility, respectively. The investigated proton energy range was 27 – 200MeV. Parts were exposed to heavy-ion beams with linear energy transfer (LET) values ranging from 2.8 to 71 MeV/(mg/cm^2).

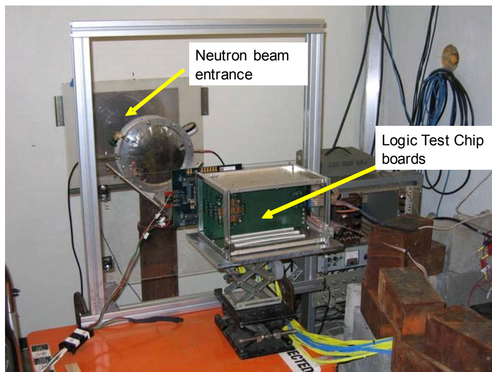

FIGURE 6. TYPICAL EXPERIMENTAL SETUP DURING ACCELERATED NEUTRON SEU TESTING IN THE ICE HOUSE AT WNR [21].

Each of the test chip designs is based on shift register topology and contains 3 inputs: Din, ClkA, ClkB and one output Dout. Each shift register consists of two identical latches: master and slave. The clock input of all of the master latches on a chip is connected to ClkA and similarly, all of the slave latches clock input is connected to ClkB[7]. In order to write a desired test pattern on a chip such as all ones, all zeros, checkerboard, etc, the Din signal is set to appropriate value (i.e. either 0 or 1) and a pulse on ClkA is applied followed by non-overlapping pulse on ClkB. Thus, writing a checkerboard test pattern (10101010…) to shift registers will result in writing 110011001100….sequence in latches of the chip. It is not possible to read both master and slave latches during one experimental run in this design. To read out the data from all the slave latches, a pulse on ClkA is applied followed by non-overlapping pulse on ClkB and data is captured from Dout output pin. Similarly, to read data from all master latches, a pulse on ClkB is applied followed by a non-overlapping pulse on ClkA.

Our test chips can be operated in two testing modes. In mode 1 devices are sensitive to charge sharing induced upsets only and in mode 2 they are sensitive to clock node strikes as well as to upsets induced by charge sharing. The test condition for charge sharing experiments is to have same polarity data stored in the latch as well as at the input pin of the latch. A required test condition for clock nodes strikes is that the data stored inside the latch should be of opposite polarity of the data at the input pin of the latch. The clock node sensitive SER testing is done by writing a checkerboard pattern, stopping the clock during the pre-defined exposure time, and after stopping the beam shifting out the content stored in master latches. The charge sharing testing is done by writing checkerboard pattern, waiting for exposure time, and reading out data from slave latches.

[7] Two non overlapping clocks to eliminate the risk of race

DESIGN TRADEOFFS

The SEUT based hardened cells are subjected to the same strict timing, area and power constraints as non-hardened designs. The design goal is to minimize timing arc changes, while minimizing the increase of area and power compared to the non-hardened cells. We have studied a wide range of SEUT drive strengths and the results of this study are summarized below. Please note that Table 2 only lists overheads for devices implemented in TC1 and TC2.

More than 95% setup and clock to out timing arcs of SEUT based cells meet the design target with average of 13% setup time degradation and 3.6% clock to out delay degradation. Only about 3.6% of the arcs are above the targeted margin. A substantial increase in routing and a corresponding increase in gate and diffusion capacitance make it prohibitively expensive to further power up the cell to bring the arcs below the allowed threshold.

The active power is estimated to increase from 40% to 150% depending on drive strength and averages at about 100%. Power consumption could be lower if the timing requirement is more relaxed. In general, smaller drive strength cells incur a higher percentage power increase. The main reason is that devices in small non-hardened cells are already close to minimum device size. Thus, device sizes are almost double in hardened cells to create redundant paths. In larger cells, devices could simply be split between two redundant paths. For the similar reasons, clock power increase is slightly higher than data power increase in terms of percentage.

The overall area overhead ranges from 50% to 180% with averages at about 100%. In general, an increase in overhead can be observed with decreasing drive strengths. As mentioned earlier and demonstrated experimentally in the next section, sufficient diffusion separation is crucial to achieving low SEU rates. However, increasing critical diffusion spacing implies cell area growth. All critical diffusions are identified through formal analysis of SEUT circuit operation and verified with circuit simulations. Shown in Table 2 are area, power and timing overheads of a typical small drive strength SEUT latch implemented in TC1 and TC2 as compared to the non-hardened control latch of the same drive strength. Also shown are the overheads for an RCC1 latch as compared to the TC1 reference latch of same drive strength.

TABLE 2 AREA, POWER AND TIMING OVERHEAD RESULTS: HARDENED COMPARED TO NON-HARDENED CELLS:

Device	Area	Active Power	Delay	Setup
Small drive strength SEUT latch	+120%	+114%	+4.9%	+11%
RCC1	+10%	+28%	+6.4%	+19%

The RCC layout technique results in modest area increases. Large cells, such as flip-flops with scan, see smaller area increases than small cells, such as a 1-read/1-write 8T register file cell. Modest power increases are also incurred due to increased diffusion capacit-

ance and interconnect capacitance. Similarly, the timing penalties are also relatively small. The power and timing estimates shown in Table 2 are based on layout extracted capacitances.

EXPERIMENTAL RESULTS AND DISCUSSION

In this section measured relative upset rates of tested SEUT and RCC devices with respect to the TC1 non-hardened reference design are presented and discussed for terrestrial and space radiation environments. SEUT and RCC SER ratios were computed by dividing the measured upset rates or cross sections with corresponding ones measured for the TC1 reference latch at the same conditions (voltage, particle energy, etc), i.e.

$$\text{SER - Ratio}_{\text{SEUT/RCC}} = \frac{\text{SER}_{\text{SEUT/RCC}}}{\text{SER}_{\text{reference latch}}} \tag{3}$$

Unless explicitly mentioned, data were collected under charge sharing conditions (not sensitive to clock node strikes) and with beams at normal incidence to the chips.

Cosmic Ray Testing Results

Despite the fact that in our typical experimental setup tens of test chips each with tens of thousands of hardened and non-hardened devices are daisy chained together, only very few upsets are detected in a typical run that can last several days at a white neutron beam facility such as WNR[8]. High-energy proton facilities (such as IUCF) are much more accessible than white neutron facilities and usually offer much higher particle beam fluxes. A good correlation between white neutron beam and high-energy proton SER results is therefore of great importance for accurate hardened device characterization and SER modeling purposes. The authors of this publication have tested several hardened test chips over the last few years and exposed them to high-energy proton and white neutron beams and in most cases observed a very good correlation. In particular for all SEUT devices reported in this work the correlation was excellent (all within error bars[9]) as illustrated in Figure 7 which compares high-energy proton (198MeV) and neutron (WNR) results for TC1 SEUT devices as a function of critical node separation.

[8] Strictly speaking, a white beam contains all energies at equal intensity. The WNR beam spectrum does not but matches that of atmospheric neutrons at sea-level. For the purposes of this paper, we continue to refer to the WNR beam as “white”

[9] All error bars in this publication denote 90% confidence levels assuming Poisson statistics

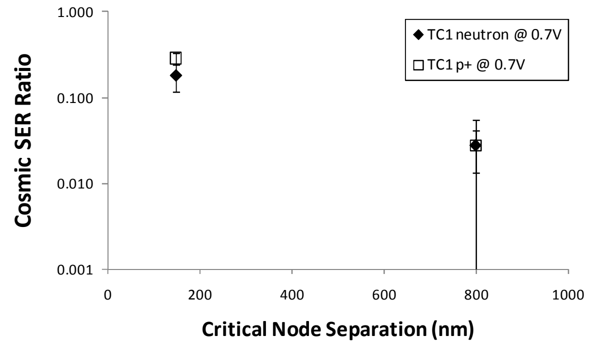

FIGURE 7. RELATIVE SER PERFORMANCE OF SEUT DEVICES AS A FUNCTION OF NODE SEPARATION UNDER 198MEV P+ AND WNR NEUTRON BEAM IRRADIATION

The fact that relative upset rates under high-energy proton and white neutron beams correlate is not surprising. We have reported in previous studies that for instance multi-cell upset (MCU) probabilities and trends of 45nm SRAMs agree as well [11]. At low proton energies MCU probabilities [11] and upset rates of SEUT devices (Figure 8) start deviating from high-energy proton and consequently from WNR neutron beam results. The physical interpretation is that, on average, the charge cloud generated by secondary particles formed in nuclear proton or neutron target nuclei (mainly Si) reactions is larger at higher incident proton or neutron energies. It also indicates that the WNR neutron beam upset cross sections for MCU and upsetting hardened SEUT devices is dominated by high-energy neutrons.

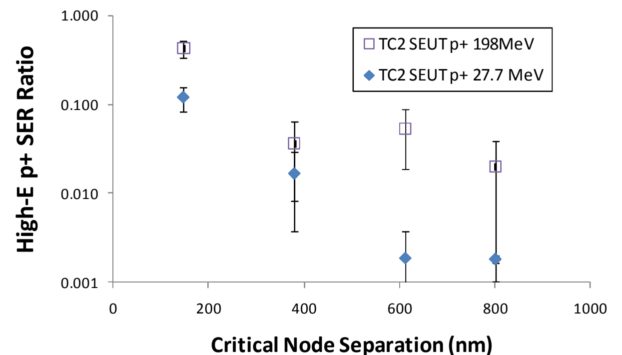

FIGURE 8. SER PROTON E-DEPENDENCE ON NODE SEPARATION FOR TC2 SEUT STRUCTURES AT 1V.

Data depicted in Figures 7-9 underline the exponential dependence of the relative SER performance of SEUT devices on critical node separation. As discussed in the design tradeoffs section, SEUT devices with relaxed node separation requirements have somewhat better power and area performance numbers and so a balance between reliability performance and cost can be struck.

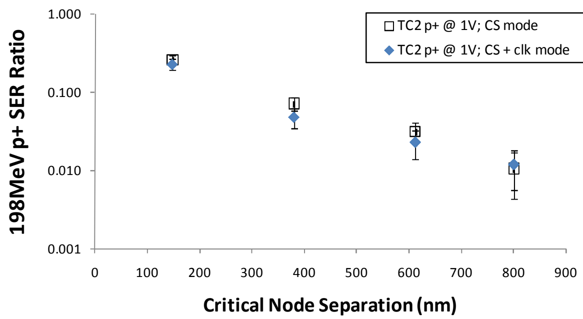

FIGURE 9. RELATIVE P+ SER PERFORMANCE OF SEUT DEVICES IMPLEMENTED ON TC2. SER RESULTS ARE SHOWN FOR CS ONLY AND CS + CLOCK NODE UPSET MODES.

All tested SEUT devices tested in this work show a low susceptibility to clock node upsets when compared to results quoted for SEUT 45nm designs reported in reference [21] (Figure 9). Even for SEUT800 devices, upset rates measured in charge sharing and charge sharing plus clock node SER testing modes are within error bars. One explanation might be that the N to P separations of diffusions located on the same clock buffers are significantly smaller in devices built in the 32nm technology than in the previously reported ones that were built in a 45nm process. Charge collected on N and P devices in the same inverter along data- or clock paths have a similar impact on SER as the layout placement of the same diffusion type (N-N or P-P) of cross-coupled inverters in memory type cell. This is consistent with data collected on 32nm test chips not discussed in this work [38].

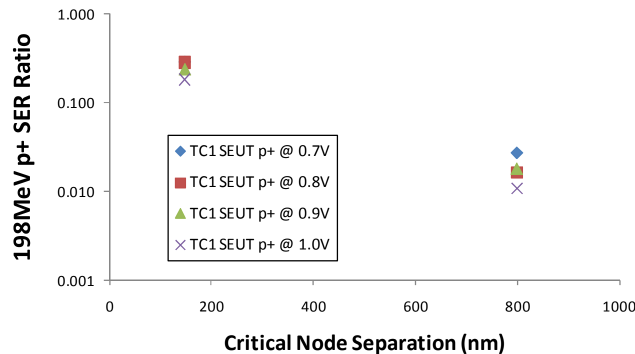

FIGURE 10. VOLTAGE DEPENDENCE OF RELATIVE SER PERFORMANCE OF SEUT DEVICES UNDER HIGH-ENERGY P+ IRRADIATION

SER benefits diminish with reduced power supply voltages for SEUT (Figure 10)[10] and RCC (Table 3) devices. Less charge (lower Qcrit at lower voltages) has a higher probability to be collected over larger distances [19] and therefore larger node separations of state weakening diffusions would be needed in both cases, SEUT and RCC, for iso-performance.

High energy proton-induced upset rates and neutron beam results also correlate for RCC type devices (Table 3). However, in the case of RCC1 the measured SER benefit was consistently higher for neutron beam testing. The authors of this work speculate that with only one poly width separation between state reinforcing diffusions, even low energy reaction products generated by low-energy neutrons deposit sufficient charge to increase Qcrit and reduce the SER susceptibility of RCC1 devices (upper line in Figure 5). In contrast, only high-energy protons or neutrons generate charge clouds large enough to result in sufficient simultaneous charge collection at state weakening diffusions that lower Qcrit[11]. In the implemented RCC designs these diffusions have separations of >300nm.

In the results summarized in Tables 3 and 5 the control latch has the same size devices as those implemented in RCC devices. However, storage node capacitances and diffusion areas are different due to differences in layout, and the addition of the dummy devices in RCC1. The SER reduction for just the capacitance and area changes is derived through SPICE simulations, and shown in the "no RCC" column. The SPICE simulation methodology has been described in detail before [36], and is not covered here. Low and high voltage measurements, and 90% CI are shown for measured data.

TABLE 3. NEUTRON AND PROTON SER RATIO RESULTS FOR RCC TYPE DEVICES

Device	**Vcc [V]**	**Neutron measured SER reduction**	**Neutron simulated SER reduction (no RCC)**	**Proton measured SER reduction**	
				27 MeV	198 MeV
RCC1	0.7	3.8x ± 30%	1.2x	2.0x ± 10%	2.5x ± 10%
RCC2	0.7	1.1x ± 30%	1.0x	1.1x ± 10%	1.3x ± 10%
RCC1	1.0	NA		NA	3.2x ± 10%
RCC2	1.0	NA		NA	1.3x ± 10%

Heavy-Ion Testing Results

Figure 11 depicts relative SER results for TC1 SEUT and RCC2 devices as a function of LET. Error bars have been omitted for better readability (except for RCC2 devices). Unfortunately no RCC1 results are available at the time of writing of this paper. At high LETs, both RCC2 and SEUT upset rates are either equal or even worse than that of the non-hardened reference latch. We expect RCC1 devices to show a somewhat better performance than RCC2 ones, but the overall benefit in heavy ion dominated orbits (such as geosynchronous ones; see below) is expected to be worse than in terrestrial radiation environments. Clock node strikes again do not seem to contribute significantly to the overall soft error rate but at the highest LET values. RCC2 performance remains poor down to the lowest LET values investigated (2.8 MeV/(mg/cm^2)).

[10] Error bars have been omitted in figure 10 to improve readability. Error bars are of the same order of magnitude as shown in Figure 9.

[11] Such as N-P devices located on opposite sides of the RCC cross-coupled devices (lower line in Figure 5)

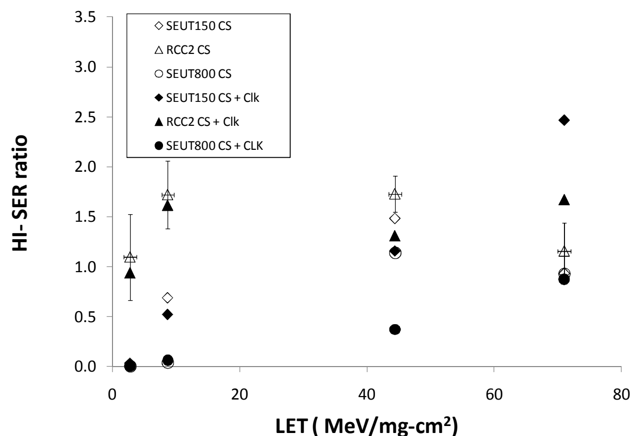

FIGURE 11. HEAVY-ION SEUT AND RCC2 RESULTS (TC1) FOR CS ONLY AND CS + CLK NODE TESTING MODES.

SER performance in geosynchronous orbits (100 mil of Aluminum shielding and solar quiet mode) has been estimated using Creme96 and results are summarized in Table 4 [37]. Please note that error bars are expected to be large[12]. Actual performance in orbit is likely worse than what is shown in Table 4, since only normal incidence data have been collected, and work by Amusan et al show that those yield optimistic results [13]. Nevertheless, performance of the only tested RCC device (RCC2) is disappointing. It is speculated that even at low to moderate LET values sufficient charge is collected at distances that cover the separation of sensitive state weakening nodes. MCU data reported in reference [11] indicate average charge cloud dimensions in excess of 1µm at high LETs which is well beyond the separation of N-P diffusions (Qcrit impact see Figure 5) in the tested RCC flavor.

TABLE 4. APPROXIMATE RELATIVE UPSET RATES IN GEOSYNCHRONOUS ORBITS (CREME96). CS + CLK NODE UPSET DATA APPLIED.

Device	SER -Ratios
SEUT150	0.64
SEUT800	0.04
RCC2	2.14

Alpha-particle Testing Results

SEUT (Figure 12) as well as RCC1 results (Table 5) demonstrate that the alpha-particle SER contribution can be neglected for typical, modern ambient alpha-particle radiation environments and fluxes. Even for SEUT150 a reduction of the order of ~200x can be expected, versus ~2-3x for high-energy proton or neutron irradiation. For SEUT devices with node separations > 600nm no upsets have been observed even after weeks of continuous testing under accelerated alpha-particle flux conditions.

[12] We have not tried to estimate 90% confidence level values of the mean for all tested devices due to the complex convolution of raw data error bars with uncertainties in non-linear fitting parameters (Weibull parameters in Creme96).

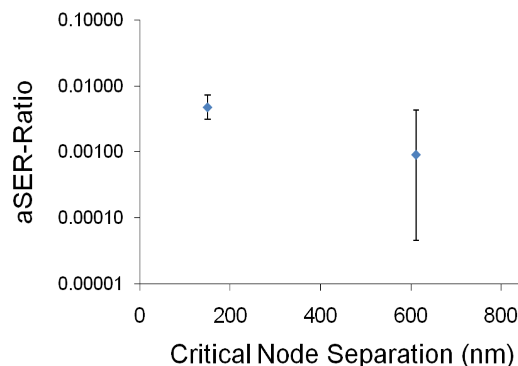

FIGURE 12. ALPHA-PARTICLE INDUCED RELATIVE SER FOR TC2 SEUT DEVICES AT 0.7V.

Alpha particle results for RCC1 and RCC2 are summarized in Table 5. The SER reduction relative to the non-RCC control latch on the same test chip is shown. The smaller separation between victim and reinforcing nodes in RCC1 results in a larger reduction compared to RCC2. The SER improvements purely due to the RCC effect are relatively modest at lower voltages. Comparing the last two columns in Table 5 for RCC1 at 0.7V yields an approximately 2x SER reduction due to the RCC effect alone. However, in real world applications, the full 10.1x SER reduction will be seen, and this includes the impact of increased capacitance and area due to the addition of dummy devices in RCC1.

TABLE 5. ALPHA-PARTICLE SER RATIO RESULTS FOR RCC TYPE DEVICES

	Voltage [V]	**Measured SER reduction**	**Simulated SER reduction due to capacitance, area changes only (no RCC)**
RCC1	0.7	10.1x ± 10%	5.0x
RCC2	0.7	2.4x ± 10%	1.5x
RCC1	1.0	57.0x	8.0x
RCC2	1.0	4.0x	3.0x

Technology Scaling Impact

The measured SEU data discussed in the previous section demonstrates that of the order of 30x SER reductions for SEUT devices and about 3x for RCC devices built in an advanced 32nm technology can be achieved with typical overheads of the order of 100% and 10%, respectively. We would like to emphasize that on the chip-level RCC might be more efficient than SEUT, despite the ~10x advantage in SER for SEUT devices. This is best illustrated by a simple example. Let’s assume the RCC SER reduction is 3x at a 20% area cost (a rather conservative assumption), whereas it is 30x for a 100% area overhead in the case of SEUT. The design goal shall be a chip-level SER reduction of y FIT. How many RCC and SEUT latches ($N_{RCC}$and N_{SEUT}) are needed to achieve this goal and what are the involved area overheads?

$$y = N_{RCC} * (x - x/3) = N_{SEUT} * (x - x/30)$$
$$=> \frac{N_{RCC}}{N_{SEUT}} = 1.45 \quad (4)$$

where x denotes non-hardend device FIT/cell. Only ~50% more RCC devices (relative to SEUT devices) are needed to achieve a chip-level SER reduction of y FIT. However, the assumed area overhead of RCC devices is 5x lower than for SEUT devices. Therefore, the overall chip-level area overhead is about 3x lower for RCC devices in the above example.

RCC fills the void where using SEUT would be over-kill. As long as there are other sources besides sequential elements contributing to the product SER[13] there is limited ROI in making all sequential elements SEUT. A better approach that leads to lower overheads but comparable SER would be to protect only highly vulnerable sequential elements with SEUT, and convert others to RCC as needed

Preserving the same absolute node separation and therefore SER benefit will be increasingly difficult and costly for SEUT type devices as we continue to scale. This will translate into more hardened devices needed to achieve the same level of SER reduction in future semiconductor technologies at a similar area overhead cost. Since the SER benefit diminishes exponentially with node separation, a corresponding larger number of hardened devices that rely on some form of local redundancy[14] would be needed. For instance, assuming simple scaling of our 32nm SEUT800 devices, the device level SER is projected to increase by roughly 3x the next few technology generations under neutron or proton radiation[15].

For RCC type designs we also expect the SER benefit at constant cost to diminish somewhat with scaling. However, the rate at what this will occur is expected to be slower than for SEUT type devices. The main reason for the expected slower rate of diminishing returns for RCC devices is based on the fact that the separation of both, reinforcing and state weakening diffusions will decrease with scaling. As long as the SER contribution due to secondary victim nodes is relatively small, technology scaling should to first order not impact the radiation robustness of this design technique (neglecting voltage scaling). In the extreme case when the impact of state weakening secondary victim nodes can be completely neglected, an improvement in SER is even expected with scaling (again, ignoring Vcc scaling).

Both hardened mitigation techniques show diminishing returns as power supply voltages are scaled, further reducing the ROI of circuit-level mitigation techniques discussed in this work.

The authors of this work do not see radiation hardened sequential elements as mutually exclusive with other SER mitigation methods, but rather as complementing in logic structures where other techniques such as parity or residue checking are not practical [18]. Placing hardened sequential elements offer a high degree of flexibility and if done correctly can yield good SER performance with little chip-level area and power tradeoffs. Although not addressed in this work, it is important to remember that an intelligent placement of hardened devices requires a solid architectural vulnerability factor (AVF) analysis of the structures of interest [18]. It would not make much sense to protect devices with very low AVF values.

[13] Such as combinational logic
[14] SEUT, BISER, DICE, circuit-level TMR, etc
[15] Assuming 0.7x scaling of distances per generation and no scaling in supply voltage (the latter assumption is very optimistic)

CONCLUSIONS

A novel circuit hardening technique called RCC (Reinforcing charge collection) is introduced. RCC exploits the fact that charge collection at state reinforcing nodes will increase Qcrit and hence reduce SER with respect to non-hardened devices of similar performance and design targets.

RCC devices and devices designed in a conventional local redundancy technique (SEUT) have been implemented on two test chips built in a 32nm bulk CMOS process. The radiation robustness of both mitigation schemes was tested for several different radiation environments. Our results indicate that even for hardened devices manufactured in such an advanced technology, SER reduction levels of the order of 30x for SEUT devices and 3x for RCC type devices can be expected for terrestrial applications. Overheads of the implemented designs are of the order of 100% for SEUT devices and 20% or less for RCC devices.

We show that RCC devices despite their modest SER reduction of ~3x, can be a more efficient mitigation technique on the chip-level. In space environments, SEUT devices are expected to fare much better than RCC based designs, however.

For SEUT devices diminishing returns are expected as we continue to scale our technologies. A somewhat better scaling performance is predicted for RCC devices. The authors believe that in the short term redundancy hardened devices will continue to play an important role for protecting few important non-arrayed architectural state elements (with high architectural vulnerability [18]), whereas RCC is a better option for protecting large numbers of logic memory elements in random logic. However, with technology and voltage scaling, both mitigation techniques are projected to eventually become inadequate and too costly.

ACKNOWLEDGEMENTS

The authors would like to thank David Parkhouse, Venkatesh Govindarajulu, Scott Lorion and Marcus Sherwin for their efforts in Test Chip design and characterization and Steven Uffner for his help with the experimental setups.

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